

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	88	703/14.ccls. and @pd>"20070701"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/12/14 18:16

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	12	ioput	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/12/14 18:18
L4	72	bidirectional adj node\$1	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/12/14 18:19

[Web](#) [Images](#) [Maps](#) [News](#) [Shopping](#) [Gmail](#) [more ▾](#)[Sign in](#)

Google

iopot simulation

Search

[Advanced Search](#)
[Preferences](#)[Web](#) [Books](#)Results 1 - 10 of about 119 for **iopot simulation**. (0.23 seconds)Did you mean: **input simulation****SIMULATION**

IOPUT. pin. behaves. like. an. input. or. output. at. a. particular. time. during. the simulation. Figure. 8. Procedure. import_iopot ...
sim.sagepub.com/cgi/reprint/60/2/79.pdf?ck=nck - [Similar pages](#)

OCRed document

at the **iopot** terminals with that group. 3.3.3 **Simulation** Algorithms Various groups comprising the. circuit axe simulated in an event driven manne.
ieeexplore.ieee.org/iel5/143/3356/00112381.pdf?arnumber=112381 - [Similar pages](#)

Hierarchical mixed-level simulation of VHDL descriptions - ASIC ...

tems, **simulation** of the circuits is needed before hard-. ware implementation. IOPUT. actual-cell in a subcell structure is a pointer ...
ieeexplore.ieee.org/iel2/3197/9098/00404583.pdf?arnumber=404583 - [Similar pages](#)
[More results from ieeexplore.ieee.org]

Hierarchical multi-level fault simulation of large systems

The approach reduces the memory requirement of the **simulation** drastically, cuit, we introduce a bidirectional type (denoted IOPUT). ...
www.springerlink.com/index/W4558586250K467H.pdf - [Similar pages](#)

Simulation Block-Diagram

iopot. Modificaions. Output. Simulated. Rern.k. [19] B. J. Karafin, "A new block diagram compiler for **simulation** of. sample-data systems,". 1965 Fall ...
doi.ieeeecomputersociety.org/10.1109/T-C.1969.222661 - [Similar pages](#)

using CAD in Design CRISP

bidirectional **iopot**. Major internal signals. are also identified. For the functional. **simulator**, the C preprocessor transforms. IEEE DESIGN & TEST ...
doi.ieeeecomputersociety.org/10.1109/MDT.1987.295162 - [Similar pages](#)

Switch-level Timing Simulation of MOS VLSI Circuits - Google Books Result

by Vasant B. Rao - 1989 - Technology - 224 pages
If a drain or source node of a pass transistor is of input strength, it is an input node to the PTB, if it is of pullup strength, it is an **iopot** (ie, ...
books.google.com/books?isbn=0898383021...

D. J. Naperville, IL ABSTRACT AIDE (Architecture Design ...

Environment) is a modeling and **simulation**. tool developed specifically all inputs and outputs (an **iopot** functions. as both). These declarations, ...
portal.acm.org/ft_gateway.cfm?id=802396&type=pdf&dl=GUIDE&dl=ACM - [Similar pages](#)

[PDF] EE_ICLAB_2000a_CB-3 Lab 3 – Behavior Level Description Oct. 11 ...

File Format: PDF/Adobe Acrobat - [View as HTML](#)
task name_of_task;. (**iopot** definition) port1;. (**iopot** definition) port2; ... 3) Choose Digital **Simulation**. 4) Verilog-XL. 5) Reference or Tutorial.
si2.ee.nctu.edu.tw/Course/ICLab/2000/ftp/lab3_note.pdf - [Similar pages](#)

[Web](#) [Images](#) [Maps](#) [News](#) [Shopping](#) [Gmail](#) [more ▾](#)[Sign in](#)

Google

iopot simulation

Search

[Advanced Search](#)
[Preferences](#)[Web](#) [Books](#)Results 1 - 10 of about 119 for **iopot simulation**. (0.13 seconds)Did you mean: **input simulation****SIMULATION**

IOPUT. pin. behaves. like. an. input. or. output. at. a. particular. time. during. the simulation. Figure. 8. Procedure. import_iopot ...
sim.sagepub.com/cgi/reprint/60/2/79.pdf?ck=nck - [Similar pages](#)

OCRed document

at the iopot terminals with that group. 3.3.3 **Simulation** Algorithms Various groups comprising the. circuit axe simulated in an event driven manne.
ieeexplore.ieee.org/iel5/143/3356/00112381.pdf?arnumber=112381 - [Similar pages](#)

Hierarchical mixed-level simulation of VHDL descriptions - ASIC ...

tems. simulation of the circuits is needed before hard-. ware implementation. IOPUT. actual-cell in a subcell structure is a pointer ...
ieeexplore.ieee.org/iel2/3197/9098/00404583.pdf?arnumber=404583 - [Similar pages](#)
[[More results from ieeexplore.ieee.org](#)]

Hierarchical multi-level fault simulation of large systems

The approach reduces the memory requirement of the simulation drastically, cuit, we introduce a bidirectional type (denoted IOPUT). ...
www.springerlink.com/index/W4558586250K467H.pdf - [Similar pages](#)

Simulation Block-Diagram

iopot. Modificaions. Output. Simulated. Rern.k. [19] B. J. Karafin, "A new block diagram compiler for simulation of. sample-data systems,". 1965 Fall ...
doi.ieeecomputersociety.org/10.1109/T-C.1969.222661 - [Similar pages](#)

using CAD in Design CRISP

bidirectional iopot. Major internal signals. are also identified. For the functional. simulator, the C preprocessor transforms. IEEE DESIGN & TEST ...
doi.ieeecomputersociety.org/10.1109/MDT.1987.295162 - [Similar pages](#)

Switch-level Timing Simulation of MOS VLSI Circuits - Google Books Result

by Vasant B. Rao - 1989 - Technology - 224 pages
If a drain or source node of a pass transistor is of input strength, it is an input node to the PTB, if it is of pullup strength, it is an iopot (ie, ...
books.google.com/books?isbn=0898383021...

D. J. Naperville, IL ABSTRACT AIDE (Architecture Design ...

Environment) is a modeling and simulation. tool developed specifically all inputs and outputs (an iopot functions. as both). These declarations, ...
portal.acm.org/ft_gateway.cfm?id=802396&type=pdf&dl=GUIDE&dl=ACM - [Similar pages](#)

[PDF] EE_ICLAB_2000a_CB-3 Lab 3 – Behavior Level Description Oct. 11 ...

File Format: PDF/Adobe Acrobat - [View as HTML](#)
task name_of_task;. (iopot definition) port1;. (iopot definition) port2; ... 3) Choose Digital Simulation. 4) Verilog-XL. 5) Reference or Tutorial.
si2.ee.nctu.edu.tw/Course/ICLab/2000/ftp/lab3_note.pdf - [Similar pages](#)


[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)

[Ad](#)
[Sc](#)
[Sc](#)

Scholar [All articles](#) - [Recent articles](#) Results 1 - 10 of about 59 for iopot simulation. (0.32 seconds)

[All Results](#)

 Did you mean: [input simulation](#)
[D Saab](#)
[R Mueller-Thun...](#)
[K Kanazawa](#)
[J Rahmeh](#)
[J Abraham](#)

[Concurrent Hierarchical and Multilevel **Simulation** of VLSI Circuits - all 3 versions »](#)

RB Mueller-Thuns, JT Rahmeh, JA Abraham, JA Wehbeh ... - **SIMULATION**, 1993 - sim.sagepub.com

... Multilevel **Simulation** of VLSI Circuits & dagger; ... This paper discusses an approach for hierarchical switch-level **simulation** of digital circuits. ...

[Related Articles](#) - [Web Search](#)

[Hierarchical multi-level fault **simulation** of large systems - all 3 versions »](#)

DG Saab, RB Mueller-Thuns, D Blaauw, JT Rahmeh, JA ... - Journal of Electronic Testing, 1990 - Springer

... For fault **simulation** one needs to keep track of the number of faults ... INPUT, OUTPUT)

entering a subcir- cuit, we introduce a bidirectional type (denoted **IOPUT**). ...

[Cited by 15](#) - [Related Articles](#) - [Web Search](#)

[Design methodology and **simulation** tools for mixed analog-digital integrated circuits](#)

R Beale, R Chadha, CF Chen, A Prosser, KM Tham - Circuits and Systems, 1990., IEEE International Symposium on, 1990 - ieeexplore.ieee.org

Page 1 Design Methodology and **Simulation** Tools for Mixed Analog-Digital Entegrated Circuits CH2868-8/90/OOOI\$() © 1990 IEEE Richard Beale, Rakesh Chadha, Chin ...

[Cited by 1](#) - [Related Articles](#) - [Web Search](#)

[Hierarchical mixed-level **simulation** of VHDL descriptions](#)

T Karnik, DG Saab, SM Kang, YK Lee, KH Kim - ASIC Conference and Exhibit, 1994. Proceedings., Seventh ... , 1994 - ieeexplore.ieee.org

... INPUT, OUTPUT or bidirectional **IOPUT**. ... The VHDL modification shown in Figure 1 for

ac- cepting MOS transistors is not implemented in the **simulator** yet. ...

[Web Search](#)

[Modeling, analysis and **simulation** of controlled rectifiers with thyristors](#)

NA Losic - Power Electronics and Drive Systems, 1995., Proceedings of ... , 1995 - ieeexplore.ieee.org

... 60/1a, and R—O.Bfl, L.SmH, V,200V, a—IF as per **iopot** file in Fig. 19 yielding wavefonma

in Fig. 20. ... Fig. 22 **Simulation** ware/noon/or ctwcit c/Fig. ...

[Web Search](#)

[Logic **simulation** with efficient deadlock avoidance by selectively suspending event data fetch based ... - all 3 versions »](#)

K Kanazawa... - US Patent 5,426,768, 1995 - Google Patents

... **iopot** terminals 116 or 126 is present, that is fetched by then execute evaluation procedures for event data the first fetch unit 3 when the **simulation** time ...


[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)

[Ad](#)
[Sc](#)
[Sc](#)

Scholar [All articles](#) - [Recent articles](#) Results 1 - 10 of about 2,980 for [bidirectional signal analog d](#)

All Results

[C Mead](#)

[J Rabaey](#)

[G Asada](#)

[J Hayes](#)

[M Dong](#)

[book] **Analog VLSI and neural systems** - [all 5 versions »](#)

C Mead - 1989 - Addison-Wesley Longman Publishing Co., Inc. Boston, MA, USA

[Cited by 1183](#) - [Related Articles](#) - [Web Search](#) - [Library Search](#)

A unified switching theory with applications to VLSI design

JP Hayes - Proceedings of the IEEE, 1982 - [ieeexplore.ieee.org](#)

... three-terminal device capable of **bidirectional signal** transmission, which ... theory only recognizes the two logic **signal** ... extensive use of both **analog** and **digital** ...

[Cited by 50](#) - [Related Articles](#) - [Web Search](#)

A wireless implantable multichannel digital neural recording system for a micromachined sieve ... - [all 4 versions »](#)

T Akin, K Najafi, RM Bradley - Solid-State Circuits, IEEE Journal of, 1998 - [ieeexplore.ieee.org](#)

... system with on-chip **analog** and **digital** ... for neurophysiological applications which combines **signal** amplification and ... A/D conversion, **bidirectional** user interface ...

[Cited by 65](#) - [Related Articles](#) - [Web Search](#)

A 12-bit sigma-delta analog-to-digital converter with a 15-MHz clock rate - [all 3 versions »](#)

R Koch, B Heise, F Eckbauer, E Engelhardt, JA ... - Solid-State Circuits, IEEE Journal of, 1986 - [ieeexplore.ieee.org](#)

... KOCH et al.: 12-BITSIGMA-DELTA ANALOG-TO-DIGITAL ... voltage *3mV **Signal/noise** 77 dB

Signal/total harmonic ... to be compatible with the **bidirectional** current sources ...

[Cited by 31](#) - [Related Articles](#) - [Web Search](#)

Verilog-AMS: Mixed-signal simulation and cross domain connect modules - [all 7 versions »](#)

P Frey, DO'Riordan - ... International Workshop on Behavioral Modeling and Simulation, 2000 - [doi.ieeeecomputersociety.org](#)

... **digital-to-analog** converters, or **bidirectional** converters, cause ... actively supports the mixed-**signal** approach, the interchange of **digital** and **analog** portions is ...

[Cited by 18](#) - [Related Articles](#) - [Web Search](#)

Boundary scan and its application to analog-digital ASIC testing in a board/system environment

PP Fasang - Custom Integrated Circuits Conference, 1989., Proceedings of ..., 1989 - [ieeexplore.ieee.org](#)

... FIGURE 5. **BIDIRECTIONAL** BOUNDARY-SCAN CELL ShiftDR ... Page 3. D. Perform logic **simulation**

of the **digital** circuit without using the **analog** input **signal(s)** but ...

[Cited by 6](#) - [Related Articles](#) - [Web Search](#)

[book] **Digital integrated circuits: a design perspective** - [all 7 versions »](#)

JM Rabaey - 1996 - Prentice-Hall, Inc. Upper Saddle River, NJ, USA

... Bobba, IN Hajj, High-performance **bidirectional** repeaters, Proceedings ... Standard


[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) | [Purchase History](#) |

Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "(iopot<and>simulation)"

Your search matched 13 of 1703577 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.



Modify Search

☐ Check to search only within this results setDisplay Format: ☒ Citation ☐ Citation & Abstract

» Search Options

[View Session History](#)[New Search](#)

» Key

IEEE JNL IEEE Journal or Magazine

IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

IEEE/IET

Books

Educational Courses

A

IEEE/IET journals, transactions, letters, magazines, conference proceedings, and

[Select All](#) [Deselect All](#)

- ☐ 1. **AIDE - A Tool for Computer Architecture Design**
Ellenberger, D.J.; Ng, Y.W.;
Design Automation, 1981. 18th Conference on
29-1 June 1981 Page(s):796 - 803
[AbstractPlus](#) | Full Text: [PDF\(672 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ 2. **On-Line Simulation of Block-Diagram Systems**
Dertouzos, M.L.; Kaliski, M.E.; Polzen, K.P.;
Computers, IEEE Transactions on
Volume C-18, Issue 4, April 1969 Page(s):333 - 342
[AbstractPlus](#) | Full Text: [PDF\(2008 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 3. **M³-a multilevel mixed-mode mixed A/D simulator**
Chadha, R.; Visweswariah, C.; Chen, C.-F.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
Volume 11, Issue 5, May 1992 Page(s):575 - 585
Digital Object Identifier 10.1109/43.127619
[AbstractPlus](#) | Full Text: [PDF\(844 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 4. **Gesture-based programming for robotics: human-augmented software a**
Voyles, R.M.; Morrow, J.D.; Khosla, P.K.;
Intelligent Systems and Their Applications, IEEE [see also IEEE Intelligent Sy
Volume 14, Issue 6, Nov.-Dec. 1999 Page(s):22 - 29
Digital Object Identifier 10.1109/5254.809564
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(672 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 5. **An Expert System Application in Semicustom VLSI Design**
Steele, R.L.;
Design Automation, 1987. 24th Conference on
28-1 June 1987 Page(s):679 - 686


[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) | [Purchase History](#) |

Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

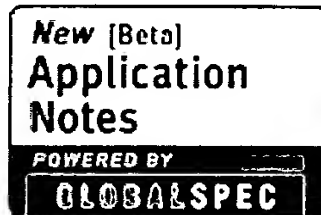
SEARCH

IEEE XPLORE GUIDE

Results for "((bidirectional signal<and>simulation)) <and> (pyr >= 1913 <and> pyr <= 2000..."

Your search matched 65 of 1703577 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.



Modify Search

((bidirectional signal<and>simulation)) <and> (pyr >= 1913 <and> pyr <= 2000)

Search

☐ Check to search only within this results set
Display Format: ☒ Citation ☐ Citation & Abstract

» Search Options

[View Session History](#)[New Search](#)

IEEE/IET

Books

Educational Courses

A

IEEE/IET journals, transactions, letters, magazines, conference proceedings, and

» Key

☒ view selected items
[Select All](#) [Deselect All](#)

IEEE JNL IEEE Journal or Magazine

IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

- ☒ 1. **A CMOS mixed signal simultaneous bidirectional signaling I/O**
Jackson, S.A.; Blalock, B.J.;
[Circuits and Systems, 1998. Proceedings. 1998 Midwest Symposium on](#)
9-12 Aug. 1998 Page(s):37 - 40
Digital Object Identifier 10.1109/MWSCAS.1998.759430
[AbstractPlus](#) | Full Text: [PDF\(64 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ 2. **An optical power equalizer based on one Er-doped fiber amplifier**
Zirngibl, M.;
[Photonics Technology Letters, IEEE](#)
Volume 4, [Issue 4](#), April 1992 Page(s):357 - 359
Digital Object Identifier 10.1109/68.127212
[AbstractPlus](#) | Full Text: [PDF\(248 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ 3. **An Experimental MOS Fault Simulation Program CSASIM**
Kawai, M.; Hayes, J.P.;
[Design Automation, 1984. 21st Conference on](#)
25-27 June 1984 Page(s):2 - 9
[AbstractPlus](#) | Full Text: [PDF\(664 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ 4. **IEEE Standard Test Interface Language (STIL) for digital test vector data**
27 Aug. 1999
[AbstractPlus](#) | Full Text: [PDF\(508 KB\)](#) IEEE STD
- ☐ 5. **1995 Index IEEE Journal of Solid-State Circuits Vol. 30**
[Solid-State Circuits, IEEE Journal of](#)
Volume 30, [Issue 12](#), Dec. 1995 Page(s):1
Digital Object Identifier 10.1109/JSSC.1995.482209
[AbstractPlus](#) | Full Text: [PDF\(3316 KB\)](#) IEEE JNL
[Rights and Permissions](#)